Another Brick in the Nanowall

Scientists, just as nano-architects would, are exploring different ways to design nanostructures with fine control over shape and position. A brand-new approach now allows one to build 2D nanowalls up by laying them down brick by brick.

Since the invention of integrated circuits by Jack S. Kilby in 1958, the ability to engineer nanoarchitectures can certainly be singled out as one of the utmost achievements of our technological era. Many alternative paths, however, are still being explored in order to achieve greater control over the shape and position of such nanoarchitectures as well as more flexibility in their constitutive materials. Gyu-Chul Yi and collaborators at POSTECH (Pohang University of Science and Technology, Gyeongbuk, Korea) have proposed a new approach to engineer nanostructures using real nanowalls, which are built brick by brick!

Just as architects do for buildings, scientists aim at building very well controlled 3D structures at the nanoscale. These *nanoarchitects* can be divided into two schools of thought: *bottom-up* vs. *top-down*. Using construction as an analogy, a wall can be raised by laying it down brick by brick — a bottom-up approach — or by pouring concrete inside a mould — a top-down approach. In a top-down approach nanosystems are constructed from larger entities without atomic-level control; for example, a microchip is realized by printing a circuit on a silicon substrate by microlithography and then by etching it in a chemical solution. In a bottom-up approach, conversely, molecular components are pieced together, relying on their chemical properties, in order to give rise to more complex systems, materials and devices.

Top-down processes are technologically predominant in nanofabrication and have been very successfully applied to the production of high-density electronic devices, such as microchips. However, one of their major limitations is that "the used materials have been restricted mainly to silicon and other polycrystalline and amorphous thin films," Yi points out, "since high quality heteroepitaxial thin film on silicon substrates are difficult to be prepared." Moreover, a heteroepitaxial growth, which is the growth of a crystalline film on a substrate of a different material, "can be easily contaminated or damaged during lithography or etching."

In order to overcome such limitations, bottom-up methods have been explored. "We believe," Yi adds, "that bottom-up approaches offer advantages in the preparation of high quality single crystal nanomaterials on many substrates including silicon, glass, and plastics." In opposition to top-down processes, however, the exact positioning of the nanostructures on the substrate, already demonstrated in 1D [1], still represents a titanic challenge in 2D.

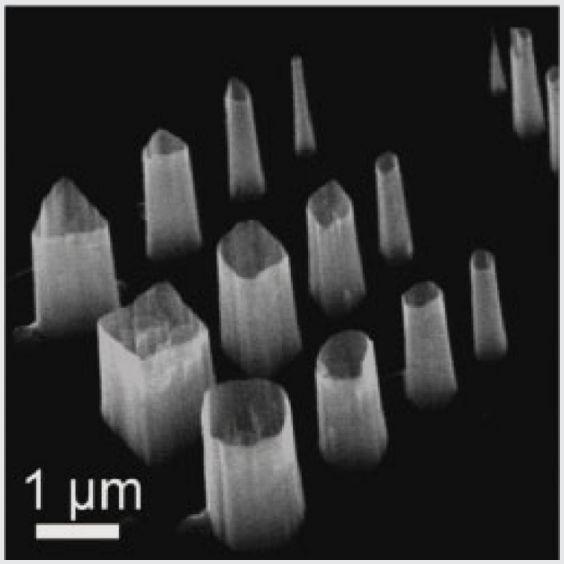

Figure 1: Brick by brick. Nanowalls with different shapes at the desired position built from the bottom-up, laying them down brick by brick. Courtesy of *Advanced Materials*.

Now, the work of this Korean group offers a solution for such a challenge. It shows the feasibility of growing 2D nanowalls at the desired location and with the desired shape on a silicon substrate, the same as those used in integrated circuit devices. "I think that the most exciting scientific core of our findings," Yi explains, "is the observation of selective formation of ZnO nanowalls along pattern edges on a GaN/Si substrate, which enabled us to control the nucleation sites in order to grow nanomaterials at specific positions." The nanowalls made of ZnO, indeed, were grown on a silicon substrate with a GaN intermediate layer. Such nanowalls will normally grow randomly on such substrate, but Yi and co-workers were able to direct their growth in 2D with a trick: some masks in SiO_2, which were laid on the substrate using conventional lithography, were the anchors for the following growth of the nanowalls.

Is it possible to adapt the same technique to different materials? "We believe that other materials can be used to grow 2D nanostructures, although we have not tried yet," Yi explains. Mark Kreuzer at ICFO (The Institute of Photonic Sciences, Barcelona, Spain) believes that bottom-up approaches may be more suited than top-down techniques in applications "where cost is an issue and the access to nanodesign tools, such as lithography, etching and thermal evaporation, is limited, or where the quality of the structure is important, for example in preparation of plasmonic sensors based on seed growth of colloids. These colloidal sensors offer optical characteristics more favourable due to the crystallinity of the metal." Also in integrated circuits, the limited materials available in top-down approaches have reduced the effective functionalities that could be implemented. So far, to date, these limitations have made it difficult to fabricate photonic-electronic integrated devices on silicon.

"Single crystal materials on different substrates could be applied to a wide range of devices, such as flexible displays, light sources, and energy conversion devices, like solar cells," Yi adds. "Moreover, these high-quality crystalline nanoarchitectures could be employed to integrate many devices, including electronic and optoelectronic nanodevices, on silicon substrates." Before coming to this stage, giving an answer to many unaddressed questions is still fundamental to lay the foundation of a bright future of applications for bottom-up strategies.

The work from the Korean group already shows the capability and flexibility of using a bottom-up approach to engineer nanostructures with precise control in shape and position. "It still necessitates the use of lithographic methods to prepare the nucleation sites," Kreuzer concludes, "but the ability to simply produce highly reproducible nanowalled structures shows a step forward in the progress of bottom-up sample preparation."

[1] W. Lu and C. M. Lieber, Nanoelectronics from the bottom up, Nat Materials 6, 841-850 (2007).

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